IN THE CLAIMS:

The current claims follow. For claims not marked as amended in this response, any difference in the claims below and the previous state of the claims is unintentional and in the nature of a typographical error.

1.   (Currently Amended) A method for supporting software pipelining, comprising:

receiving a shift mask signal from a shift mask register having information on a shifting region of a register file, wherein the shifting region comprises a plurality of non-contiguous registers;

receiving a shift signal from an external component to trigger a shift;

identifying a shifting register queue based on the shift mask signal, wherein the shifting register queue comprises a plurality of queue registers; and

shifting the contents of the queue registers based on the shift signal such that each register in the shifting register queue receives the contents of the previous register in the shifting register queue.

2.   (Previously Presented)   The method of Claim 1, wherein the shift mask signal is received from a shift mask register associated with the shifting register queue.

3.   (Previously Presented)   The method of Claim 1, wherein the shift signal is received from an external component.

4.   (Previously Presented)   The method of Claim 1, wherein the register file comprises the plurality of queue registers and a plurality of non-queue registers, and wherein the shift mask signal comprises a plurality of bits, each bit associated with a corresponding register in the register file.

5.   (Previously Presented)   The method of Claim 4, wherein the bits in the shift mask signal that comprise 1s correspond to the queue registers, and wherein the bits in the shift mask signal that comprise 0s correspond to the non-queue registers.

6.   (Previously Presented)   The method of Claim 4, wherein the bits in the shift mask signal that comprise 0s correspond to the queue registers, and wherein the bits in the shift mask signal that comprise 1s correspond to the non-queue registers.

7.   (Currently Amended) A system for supporting ~~software~~ pipelining comprising:

a register file embodied in a computer readable medium comprising:

a plurality of queue registers forming a shifting register queue based on a shift mask signal having information on a non-contiguous shifting region of the register file; and

at least one non-queue register located between two queue registers.

8.   (Original)   The system of Claim 7, further comprising a shift mask register operable to identify the queue registers within the register file.

9.   (Previously Presented)   The system of Claim 8, wherein the shift mask register

is further operable to provide the shift mask signal to the register file to identify the queue registers

for the register file.

10.   (Previously Presented)   The system of Claim 7, wherein the register file further

comprises:

write decoding logic operable to generate control signals and write signals; and

a plurality of multiplexers, wherein each multiplexer corresponds to a register within the

register file and is operable to receive one of the control signals from the write decoding logic and is

further operable to provide write data to the corresponding register based on the control signal.

11.   (Previously Presented)   The system of Claim 10, wherein the registers within

the register file comprises edge-triggered flip-flops and are operable to receive the write data from

the multiplexer and to receive one of the write signals from the write decoding logic.

12.   (Previously Presented)   The system of Claim 11, wherein for each register other

than a first register, the write data provided by each multiplexer to the corresponding register based

on the control signal comprises data from a previous register in the register file.

13.   (Currently Amended) A system for supporting ~~software~~ pipelining comprising:

a register file <u>embodied in a computer readable medium</u> ~~operable~~ <u>configured</u> to receive a shift mask signal and a shift signal, to identify a shifting register queue having a plurality of <u>non-contiguous</u> queue registers within the register file based on the shift mask signal, and to shift the contents of the queue registers based on the shift signal.

14.   (Original)   The system of Claim 13, further comprising a shift mask register operable to identify the queue registers within the register file.

15.   (Previously Presented)   The system of Claim 14, wherein the shift mask register is further operable to provide the shift mask signal to the register file.

16.   (Previously Presented)   The system of Claim 13, wherein the shift mask signal comprises a plurality of bits, wherein each bit is associated with a corresponding register in the register file.

17.   (Previously Presented)   The system of Claim 13, wherein the register file further comprises:

write decoding logic operable to generate control signals and write signals; and

a plurality of multiplexers, wherein each multiplexer corresponds to a register within the register file and is operable to receive one of the control signals from the write decoding logic and to provide write data to the corresponding register based on the control signal.

18.   (Previously Presented)   The system of Claim 17, wherein the registers within the register file comprises edge-triggered flip-flops, and wherein each register is operable to receive the write data from the multiplexer and to receive one of the write signals from the write decoding logic.

19.   (Previously Presented)   The system of Claim 18, wherein for each register other than a first register, the write data provided by each multiplexer to the corresponding register based on the control signal comprises data from a previous register in the register file.

20.   (Previously Presented)   The system of Claim 13, wherein the register file is operable to receive the shift signal from an external component.